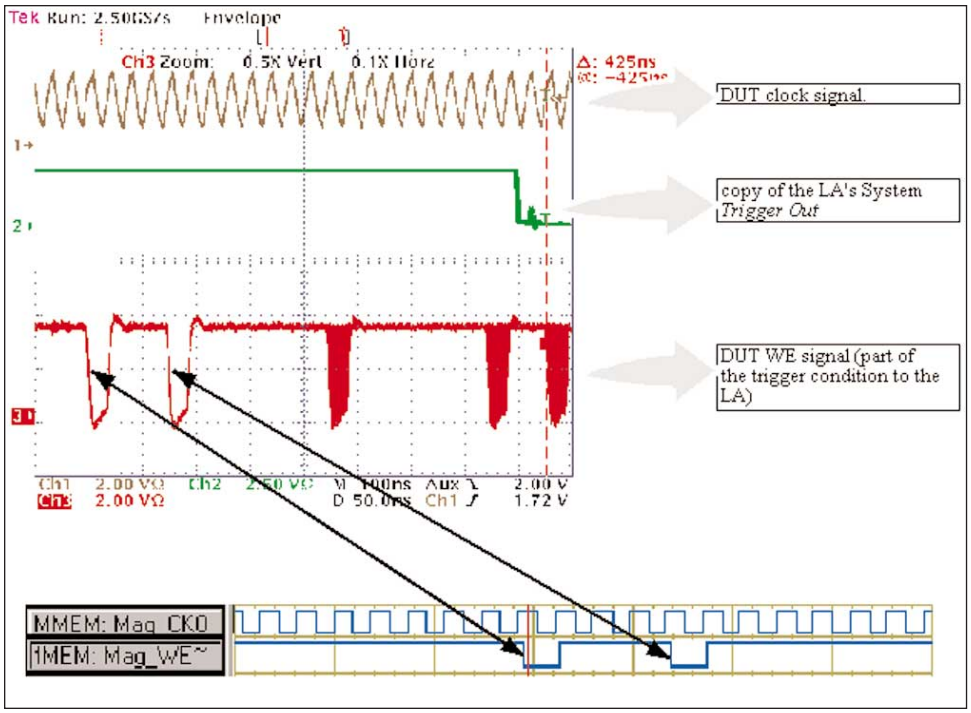
Tektronix

Application Note

Cross Triggering a TDS 694C with a TLA 700



Why Cross Trigger?

Modern digital storage oscilloscopes (DSOs) have been optimized for precise timing measurements on high-speed digital logic. The Tektronix TDS 694C, for example, provides ±15 ps accuracy in signal edge to signal edge timing measurements. This high accuracy is achieved by an acquisition system that provides a maximum sample rate of 10 GS/s per channel. With its standard 3 GHz trigger bandwidth, the TDS 694C can also trigger on very fast signal events. It cannot, however, trigger on a 64-bit wide bus address.

The TLA 700 Logic Analyzer, on the other hand, has the ability to capture and display up to 680 logic signal inputs simultaneously. Using sophisticated trigger circuitry called a trigger state machine, the TLA 700 Series can evaluate several "If-Then-Else" conditions at the same time. It can evaluate complex combinations of events and execute an extensive combination of actions; or it can capture specific events, such as memory read or write operations.

The TLA's MagniVu™ technology allows timing analysis on all input signals with a resolution of 500 ps. To do even more precise timing, the TLA7E2 and TLA7E1 DSO modules provide analog signal acquisition with 1 GHz analog bandwidth and up to 5 GS/s sample rate on each channel. The DSO module can be triggered from the TLA's digital acquisition modules and the digital modules can be triggered from the DSO module. Using the digital and DSO modules in a TLA 700, time correlation between digital and analog events can be accomplished.

However, for many of today's high-speed logic signals the 1 GHz bandwidth of the DSO module limits the accuracy of the timing measurements. For the highest performance timing measurements, it is often necessary to use a stand-alone DSO, such as the TDS 694C, with higher bandwidth and sample rate performance.

By cross triggering the TDS 694C with the TLA 700, the user can take advantage of the best attributes of both to obtain precise timing measurements.

Connecting the TLA 700 and TDS 694C for Cross Triggering

The System Trig Out signal forms the basis for synchronizing the timing measurements of the logic analyzer and the oscilloscope. Each time a trigger event occurs within the TLA 700, this active low, TTL-compatible output signal is asserted (see Figure 1). It remains asserted until the TLA memory is filled or the trigger engine is reset.

The output signal, however, does not occur simultaneously with the TLA trigger event. There can be 300 to 500 ns of delay between the time the trigger state machine recognizes an event and the time the output pulse is generated. (Note: For accurate timing measurements, this delay, and any delays in the cable connecting the TLA to the TDS, should be characterized before cross triggering. See **Trigger Delay Characterization** which follows.)

System Trig Out is available at a BNC connector on the TLA 714 or on a SMB connector on the front panel of the TLA 720 controller module. The TLA 720 includes a P6041 probe that can be used to bring the signal to a BNC connector. Use a coaxial cable to connect System Trig Out to the Aux Trigger Input on the rear panel of the TDS 694C (Figures 2 and 3).

Trigger Delay Characterization

When the connections have been made, a trigger delay characterization should be performed. Measuring the delay between the TLA's system trigger and the arrival of the System Trig Out pulse at the DSO's Aux Trigger Input ensures that accurate and time-correlated measurements will be possible.

Install a deskew fixture onto the TDS 694C probe compensation pins and connect a P6249 probe to Channel 1. With the probe attached to one set of square pins on the deskew fixture, attach one data channel from the TLA to another set on the deskew fixture. The TLA trigger threshold should be set to 0.25 V of the rising edge of the attached data line. Then, using a short record length and continuous run, the TLA can be started.

On the TDS 694C, press SAVE/RECALL SETUP > Recall Factory Setup > OK Confirm Factory Init. Set the Channel 1 vertical scale to 200 mV/div and the horizontal scale to 200 ns/div. Then set the trigger to TLA Cross Trigger (see Figure 4). In the Trigger Menu, set the mode and holdoff to Normal, and the trigger type to the negative slope edge.

Adjust the TLA Cross Trigger delay until the rising edge of the signal is at the center of the graticule. Increase the TDS 694C's horizontal scale to a faster time/div setting while adjusting the TLA Cross Trigger delay to keep the rising edge of the signal at the center. At the faster time/div settings, the jitter on the TLA Logic analyzer system trigger will cause the TDS 694C to jitter several nanoseconds. The TLA Cross Trigger delay should be adjusted to cause the range of the jitter to be centered on the center graticule position.

When this characterization has been completed, the record length, sample rate, and trigger position can all be varied without affecting the relation of the system trigger position indicated on the TLA with the trigger position on the TDS. The TLA Cross Trigger delay value will not be changed by recalling setups.

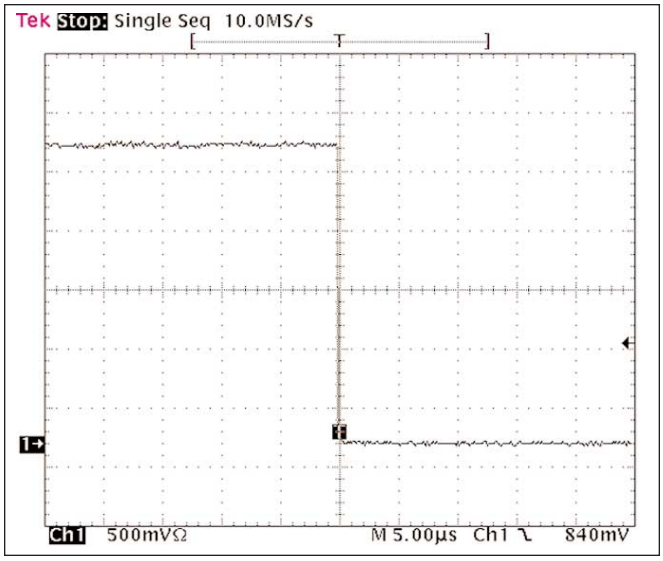


Figure 1. TDS capture of TLA System Trig Out.

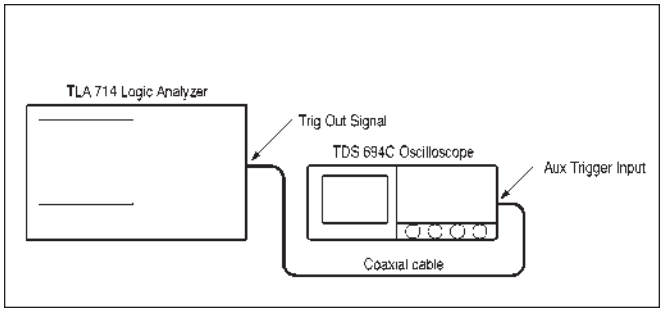


Figure 2. Block diagram of TLA 714 hookup.

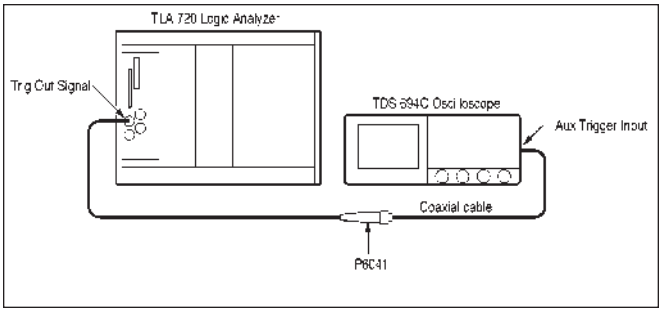


Figure 3. Block diagram of TLA 720 hookup.

Synchronizing the TDS with the System Clock

In many applications, the logic analyzer is synchronized to the system clock of the device under test. In this configuration, only events that occur on the active edges of the clock are captured. When using the TDS 694C and the TLA 700 to make timing measurements on a synchronous system, it may be desirable to synchronize the TDS trigger with both the TLA trigger and the device's system clock.

This synchronization can be easily accomplished if the clock is connected to a TDS input channel. Then, using the delayed trigger capability of the TDS, acquisitions can be synchronized with the TLA trigger event and the system clock edge. Figure 5 shows a sample TDS acquisition synchronized to the system clock. Notice the main and delayed trigger icons below the waveform display.

The trigger setup for this acquisition was set to TLA Cross Trigger for the main TDS trigger. The system clock (Channel 4) was used to trigger the delayed trigger of the TDS 694C. With this setup, all TDS acquisitions are captured when the TLA trigger occurs followed by a rising edge on the clock.

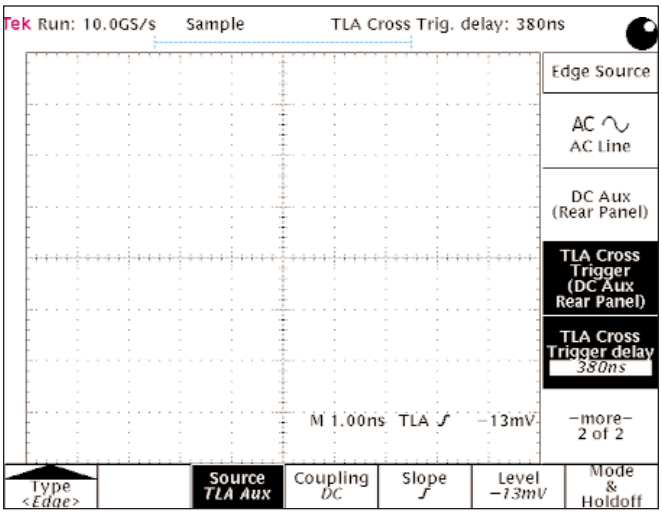


Figure 4. TLA Cross Trigger Source Menu.

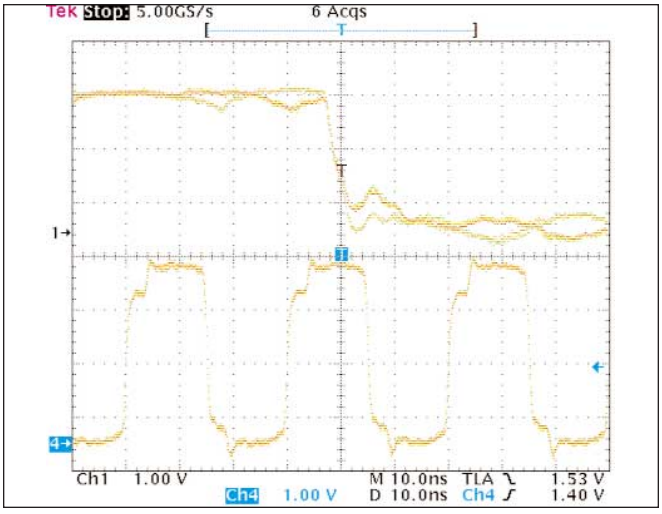


Figure 5. TDS acquisition synchronized with the System Clock.

Typical Cross Trigger Applications

Measuring Setup and Hold Timing on a Synchronous Bus

When setup and hold times are 1 ns or less, the resolution of the TLA 700's MagniVu technology (500 ps) may not be enough to identify marginal timing. For more precise measurements, the TDS 694C can be used to observe 2 or 3 data lines along with the clock signal.

Triggering on Specific Events

In logic circuit design, having the ability to trigger a DSO on specific events will often speed up debugging. Most modern DSOs have the ability to trigger on a logic pattern of up to 4 bits, but that isn't always enough. The TLA 700's logic state machine can observe hundreds of signals simultaneously and can evaluate up to sixteen trigger states with complex expressions, like "If-Then-Else" clauses.

Using the TLA 700 as the trigger for the TDS 694C gives the user the ability to filter events captured and viewed on the scope so that the measurements performed are done just on the events of interest.

Characterizing Device Performance

The 500 ps timing resolution of the TLA 700's MagniVu™ technology is not always enough to completely characterize device performance in today's high-speed designs. Using the TLA to trigger the TDS 694C allows the user to find the bus cycles of interest using multi-channel TLA triggering. The user can then zoom in with less than 15 ps timing resolution on all four signals observed with the TDS.

In addition, the acquisition system of the TLA is inherently two-dimensional (voltage vs. time). For some timing and characterization measurements, a third statistical dimension is often useful. The TDS 694C allows a user to statistically characterize an edge, pulse width, or clock period using histograms and measurement statistics. Using statistical calculations, timing errors due to clock jitter, for example, can be accurately measured.

Verifying Timing Relationships

For many logic design applications, four channels on a DSO are not enough. In DRAM interface designs, for example, the timing relationships of signals such as RAS, CAS, CS, clock, and data must be verified. Using the TLA 700 and MagniVu technology, all of these signals can be measured with 500 ps resolution. Then if a problem is suspected on any four of the signals, the TLA can be used to trigger the TDS 694C for greater timing resolution (less than 15 ps).

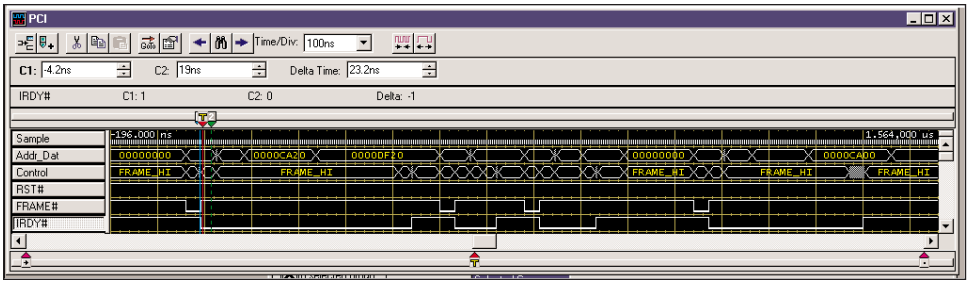


Figure 6. TLA Capture of the 64-bit bus.

Measurements of a High-speed Design with Cross Trigger

The following describes how cross triggering the TDS 694C with the TLA 700 can be used to characterize timing on a 64-bit PCI bus. With the TLA 700, activity on the PCI bus was captured synchronous to the bus clock (CLK) (Figure 6).

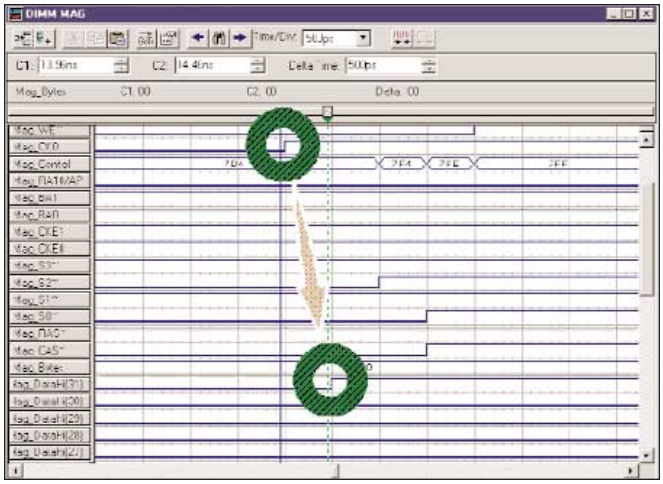


Figure 7. MagniVu used to observe the Data and Clock Timing.

Using MagniVu on the TLA, the setup and hold time of data lines on the bus were verified. However, a few signals in the system showed setup or hold times that were close to the 1 ns system margin. These signals are highlighted in Figure 7.

Data on bit 31, as displayed by the TLA, shows a hold time of 500 ps. This hold time would violate the 1 ns minimum system specification and needs to be verified with a DSO.

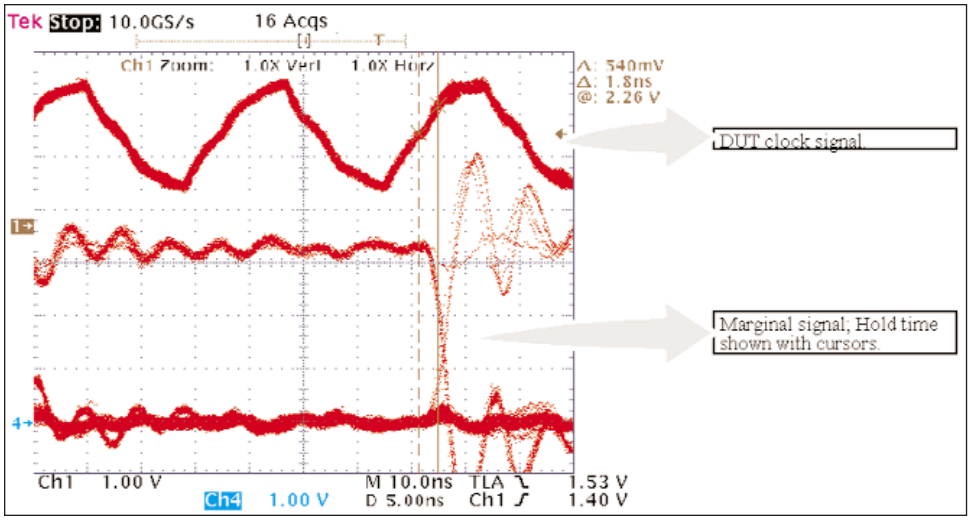


Figure 8. Measuring the data line with the TDS 694C.

Using the DSO to look at data bit 31 relative to the clock could normally be done independent of the TLA trigger. However in this case, other events on the data line tend to confuse and blur the view of the problem. By using the TLA to trigger the TDS, only bus cycles of interest are captured and a clearer picture of what is happening is possible. Figure 8 shows a measurement of the data line with the TDS 694C DSO. The more accurate timing resolution of the oscilloscope indicates the signal is within the 1 ns hold specification.

Conclusion

The Cross Trigger feature of the Tektronix TDS 694C allows digital designers to combine the strengths of the DSO with the strengths of the logic analyzer. The setup and connection of the TDS and TLA in order to cross trigger is simple, but should be carefully characterized in order to maximize timing precision. The example measurement described here is only the start of the many possibilities for the TDS cross triggering capability. There are many applications in which cross triggering a TDS 694C with a TLA 700 Logic Analyzer will produce more accurate timing measurements (see sidebar **Typical Cross Trigger Applications**).

For further information, contact Tektronix:

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